Remarks

Applicants respectfully request reconsideration of the present U.S. Patent application as amended herein. Claims 1, 7, 12 and 25 have been amended. Claim 6 has been canceled herein. Claims 17-24 have been canceled previously. No claims have been added or canceled herein. Thus, claims 1-16 and 25-29 are pending.

Claims 1, 2, 6-8, 12, 13, 25 and 26 were rejected as being unpatentable over U.S. Patent No. 6,909,645 issued to Eilert (*Eilert*) in view of U.S. Patent Publication No. 2007/0088904 of Sinclair (*Sinclair*) and further in view of U.S. Patent No. 7,389,395 issued to Garthwaite, et al. (*Garthwaite*). Claim 6 has been canceled. Therefore, the rejection of claim 6 is moot. For at least the reasons set forth below, Applicants submit that claims 1, 2, 7, 8, 12, 13, 25 and 26 are not rendered obvious by *Eilert*, *Sinclair* and *Garthwaite*.

Claim 1 recites:

> an array of memory locations implemented as bit-alterable, non-volatile phase change memory configured as a plurality of blocks of memory locations; and
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> control circuitry coupled with the array of memory locations to cause a segment of data to be stored in the array of memory in logically adjacent memory locations spanning a boundary between a first block of memory locations and a second block of memory locations, wherein the block of data has only one corresponding header, ***wherein the segment of data comprises system data to be used during system initialization and further wherein the segment of data is stored in a pre-selected location within the memory array for all initialization sequences.***

Thus, Applicants claim storing data in adjacent memory locations of bit-alterable, non-volatile memory that span a memory boundary with a single header. Further, the segment of data comprises system data to be used during system initialization and further wherein the segment of data is stored in a pre-selected location within the memory array for all

initialization sequences. Note that the memory is configured as a plurality of blocks of memory locations. Claim 25 recites similar limitations.

Eilert discloses bit-alterable, non-volatile memory. However, *Eilert* does not disclose storing data in adjacent memory locations of bit-alterable, non-volatile memory that span a memory boundary with a single header with system data in pre-selected locations in the bit-alterable memory. *Sinclair* discloses a flash memory system in which a block of data may be stored across multiple memory segments. However, *Sinclair* does not provide the reduced overhead as recited in the claims. See paragraph 0051. Eilert discloses initialization data stored in ***ROM***, but not bit-alterable memory. Therefore, no combination of *Eilert* and *Sinclair* can teach or suggest the invention as recited in claims 1 and 25.

Claim 2 depends from claim 1. Claim 26 depends from claim 25. Because dependent claims include the limitations from which they depend, Applicants submit that claims 2 and 26 are not rendered obvious by *Eilert*, *Sinclair* and *Garthwaite* for at least the reasons set forth above.

Claim 7 recites:

> receiving data to be stored in a bit-alterable, non-volatile phase change memory configured as a plurality of blocks of memory locations; and
>
> causing the data to be stored as at least one data fragment in logically adjacent memory locations that spans a boundary between a first block of memory locations and a second block of memory locations, wherein the block of data has only one corresponding header, ***wherein the data fragment comprises system data to be used during system initialization and further wherein the data fragment is stored in a pre-selected location within the memory array for all initialization sequences***.

Thus, Applicants claim storing data in adjacent memory locations of bit-alterable, non-volatile memory that span a memory boundary with a single header. Further, the segment of data comprises system data to be used during system initialization and further wherein the segment of data is stored in a pre-selected location within the memory array for all initialization sequences. Note that the memory is configured as a plurality of blocks of memory locations. Claim 12 recites similar limitations.

As discussed above, no combination of *Eilert*, *Sinclair* and *Garthwaite* teaches or suggests storing initialization data in adjacent memory locations of bit-alterable, non-volatile memory that span a memory block boundary with a single header. Therefore, no combination of *Eilert*, *Sinclair* and *Garthwaite* can teach or suggest the invention as recited in claims 7 and 12.

Claim 8 depends from claim 7 and claim 13 depends from claim 12. Because dependent claims include the limitations from which they depend, Applicants submit that claims 7 and 12 are not rendered obvious by *Eilert*, *Sinclair* and *Garthwaite* for at least the reasons set forth above.

Claims 3-5, 9-11, 14-16 and 27-29 were rejected as being unpatentable over *Eilert*, *Sinclair* and *Garthwaite* in view of U.S. Patent Publication No. 2006/0245236 of Zaidi (*Zaidi*). For at least the reasons set forth below, Applicants submit that claims 3-5, 9-11, 14-16 and 27-29 are not rendered obvious by *Eilert*, *Sinclair, Garthwaite* and *Zaidi*.

Claims 3-5, 9-11, 14-16 and 27-29 depend from independent claims discussed above. *Zaidi* is cited to teach phase change memory with chalcogenide material. Whether or not this is an accurate characterization of *Zaidi*, *Zaidi* fails to cure the deficiencies of *Eilert*, *Sinclair* and *Garthwaite* discussed above. Therefore, no

combination of *Eilert*, *Sinclair, Garthwaite* and *Zaidi* can teach or suggest the invention as recited in claims 3-5, 9-11, 14-16 and 27-29.

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 1-5, 7-16 and 25-29 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application. Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

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/Paul A. Mendonsa/
Paul A. Mendonsa
Attorney for Applicant
Reg. No. 42,879

1279 Oakmead Parkway
Sunnyvale, CA 4085-4040
(503) 439-8778